The ALICE silicon pixel detector read-out electronics

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Abstract

The ALICE silicon pixel detector (SPD) constitutes the two innermost layers of the ALICE inner tracker system [1]. The SPD contains 10 million pixels segmented in 120 detector modules (half staves), which are connected to the off-detector electronics with bidirectional optical links. Raw data from the on-detector electronics are sent to 20 FPGA-based processor cards (Routers) each carrying three 2-channel link-receiver daughter-cards. The routers process the data and send them to the ALICE DAQ system via the ALICE detector data link (DDL). The SPD control, configuration and data monitoring is performed via the VME interface of the routers.

This paper describes the detector readout and control via the off-detector electronics.

I. Introduction

The ALICE silicon pixel detector (SPD) constitutes the two innermost layers of the ALICE inner tracker system which contains 10 million pixels organized in 120 detector modules called half-staves. Each half stave consists of a linear array of 10 ALICE pixel chips bump bonded to two silicon sensors and is read out using a multi-chip module (MCM) [2-5]. The ALICE trigger has three stages (L0, L1, L2) whereas the SPD system uses L1 and L2 triggers only. The pixel chips provide binary hit information, which is stored in a delay line during the L1 decision time. In case of a positive L1 decision the hit is stored in one out of four multi-event buffers where the data wait for the L2 decision to be read out or discarded. The ALICE trigger scheme foresees a non-pipelined architecture and allows the detector read-out systems to temporarily reject triggers by sending a busy signal to the central trigger processor. The ALICE SPD off-detector electronics controls, configures and reads out the detector via bidirectional optical links. The front-end data streams are processed in 20 readout modules (Router), based on FPGAs, each carrying three 2-channel link-receiver daughter cards. The processed data are sent to the ALICE-DAQ system on the ALICE detector link (DDL) for permanent storage. The SPD control, configuration and data monitoring are performed using the VME interface of the routers. In Table 1 are summarized main system parameters for SPD.

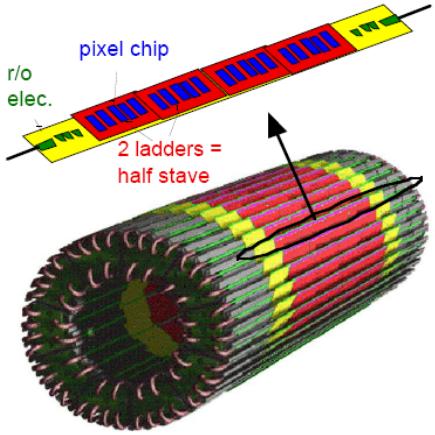

Figure 1: Silicon Pixel Detector

A. Main system parameters of SPD

The main system parameters of SPD are in Table 1.

Table 1: Main system parameters

L1 rate	1 kHz
L1 latency	6.5 μs
L2 rate	40–800Hz
L2 latency	100 – 500 μs
Read-out time	256 μs
Multi-event buffers	4
Total Ionizing Dose (inner layer)	2.5 kGy (10 years)
Fluence (1MeV equivalent)	$3x10^{12}cm^{-2}$(10 years)
Material budget per layer	<1% X_0

B. General readout scheme

Configuration and trigger data are sent from the VME based electronics (router and link receiver card) in the control room to the on-detector electronics via two optical fibers, one carrying the clock and one carrying serial data. On the detector the PIN diodes in the optical package and the RX40 chip [6] convert the optical signals to electrical signals. The PILOT2003 chip [7,8] initiates the read-out of the pixel chips and controls the ANAPIL chip, which provides analog bias voltages to the pixel chips and measures supply, bias voltages

and the temperature on the detector. Once read-out has been initiated the nonzero-suppressed data are sent from the pixel chips via the PILOT2003 [18] and an 800 Mbit/s G-link compatible optical link driver chip GOL [9,10] and an optical fiber to the control room. The description of row data format is in [16]. There the data are zero-suppressed and formatted in the FPGA-based link receiver mezzanine board. Three such boards, each one serving 2 data channels, are located on one router module. The router performs data multiplexing and establishes the interface to the ALICE trigger and data acquisition. In total 20 router cards read out the 120 half staves. Figure. 2 shows a block diagram of the full SPD read-out chain.

One ALICE standard detector data link DDL [11] per router is used to transmit the data stream to the ALICE DAQ [12,19]. The data are read-out from the link receivers and stored in the FIFO memory inside Router FPGA which is connected to one DDL module. When the DAQ is ready data are immediately sent through the FIFO and DDL module to the DAQ. If the DAQ in not ready data are stored in the FIFO and it waits until the DAQ will be ready.

The Router communicates with the Detector Control System (DCS) through the VME bus. The SPD DCS monitors the read out electronics and the detector services. For monitoring purpose the DCS can read dual-port memory on the Router where samples of data flowing to DAQ are stored. The DCS is responsible for the detector configuration.

In the Router FPGA 6 independent JTAG controllers are implemented. Each controller sends configuration data to the pixel detector. The controllers can run in parallel so that the data are sent to all channels simultaneously.

It is possible to load new code to adapt data processing capabilities to any possible new requirements into FPGAs and EPROMs through remote programming based on JAM player software and the VME access to the Router.

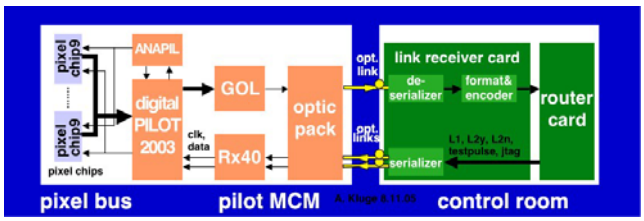

Figure 2: Global readout block diagram

II. LINK RECEIVER

Each of the two link-receiver channels has three optical fibre links; two links for the clock and the serial trigger, control and configuration data and one 800 Mbit/s G-link compatible link to receive data from the detector.

On the link receiver the pixel data stream from the detector is de-serialized, the received data is checked for format errors and the data are stored in a buffer-FIFO before data are zero suppressed, encoded, re-formatted and written to a dual port memory. When all data from one event are stored in the dual port memory on the link receiver, the link receiver asserts event ready flag to be read out by Router processor. The Link receiver also asserts to the Router processor the error flags, that are identified in the data stream coming from detector, like busy violation, idle violation, Glink down error, Glink transmission error, FIFO overflow, memory overflow, Single Event Upset (SEU) error, control error, control detector feedback error and control pixel error. Busy violation is asserted when a 5th L1 trigger signal has been received by the on detector electronics, although all (4) multi event buffers were full and the corresponding busy signal (which has been sent to the trigger) has been active. Idle violation is asserted when a L2 signal (either L2y or L2n) has been received by the on detector electronics although no corresponding L1 signal has been received. Glink down error is asserted when the data link was down during the event read out. The Glink transmission error is asserted when Glink receiver found a error in transmission protocol during the readout of the corresponding event. The FIFO overflow is asserted when at least one of the pixel converter readout FIFOs was full at least once during the data read out. The memory overflow is asserted when at least one of the pixel converter readout memories was full at least once during the data read out. SEU error is asserted when it was detected and was not recovered by the on detector electronics. The control error is asserted when in the control link (from the control room to the detector) a transmission error occurred between the precedent and the actual read out of the corresponding event. All control signals sent to the detector (L1, L2y, L2n, test signal, JTAG signals) are sent back on the fast link for error detection. The control detector feedback error is active if one of the signals sent to the detector was not received back between the precedent and the actual event read out. The control pixel error is asserted when error occurred on the pixel chips. . This error information is sent to the DAQ together with event data in DAQ header.

The G-link receiver deserializes the data stream and recovers the 40 MHz transmission clock using a commercial component (Agilent HDMP1034) [16]. The implementation of the link receiver is also based on a commercial FPGA and dual port memories. Figure 3 shows a block diagram of the link receiver. The expected occupancy of the detector will not exceed 2%. It is therefore efficient to encode the raw data format after zero suppression. In the raw data format the position of a hit within a pixel row is given by the position of logic '1' within a 32-bit word. The encoder transforms the hit position into a 5-bit word giving the position as a binary number for each single hit and attaches chip and row number to the data entry. The output data from the FIFO are encoded and stored in an event memory in a data format complying with the ALICE DAQ format [13].

Figure 3: Block diagram of the link receiver

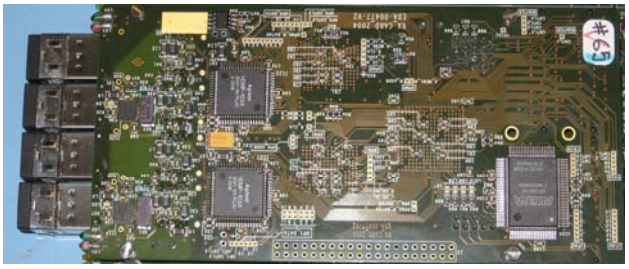
Figure 4: Link receiver (transceiver)

III. ROUTER

The Routers receives the trigger control signals from the ALICE Central Trigger Processor (CTP) through the on-board TTCrx chip [14] and forwards the trigger commands to the pixel detector. Upon reception of the L1 trigger signal the Router sends trigger signals to the detector and the pixel data are copied into multi-event buffers on the pixel chips. After reception of the positive L2 decision, the Router starts to check the event ready flag in the status register of the link receivers. When event ready flag appears the router processor reads the data from the link receiver dual port memory.

Each Router sequentially reads one event from each of the link receiver channels in order to merge data from the 6 channels and labels them with trigger and status information to build one router sub event. The sub events of each of the routers are sent to the ALICE-DAQ system through the ALICE detector data link (DDL). The read out data stream can also be copied into a dual port memory, where it is accessible for data monitoring and analysis via the VME-interface. The Router architecture is shown on Figure 5.

The data access for the SPD control and configuration is performed via the router VME-interface. The router converts the data to JTAG compatible commands which are sent to the detector through the optical links with a maximum data rate of 5 Mbit/s.

The Router is a 10-layers Printed Circuit Board with a 1020 pins chip Altera Stratix EP1S30 component as main processor. The VME interface is inside an Altera APEX EP20K60EQC FPGA with 240 pins.

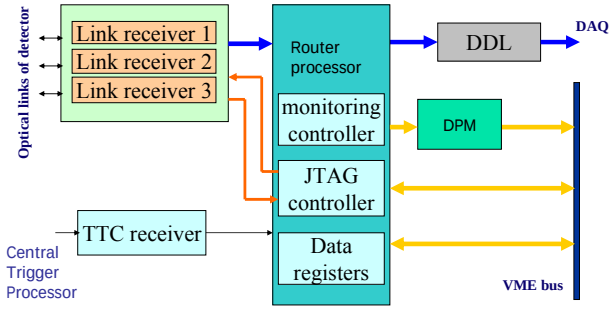

Figure 5: Router architecture

A. JTAG controller for the configuration of the pixel readout chips

For the pixel readout chip configuration a specific JTAG controller is used. Each Router has 6 independent JTAG controllers: one each channel serving one half-stave. It works with macro instructions which are stored in the input FIFO memory. Upon receiving the command "execute start" from VME bus, the JTAG controller starts to read data from the input FIFO memory processes the required operations i.e. sends appropriate TCK, TMS, TDI signals to the pixels chips and stores the data received from pixel chips i.e. stores TDO signals to the output FIFO. The data from the output FIFO can be read-out via VME bus. All 6 channels can be programmed with the same data in parallel. The format of the JTAG controller data is described in [15].

B. Remote programming

The Router and the link receivers employ ALTERA FPGAs and EPROMs only. This allows to use ALTERA JAM player software for remote programming of these devices. All these devices are in one JTAG chain (Figure 6) and can be programmed remotely using the JAM player software and the JAM player logic inside the VME FPGA. The VME FPGA cannot be programmed because it is used as driver for the JTAG chain.

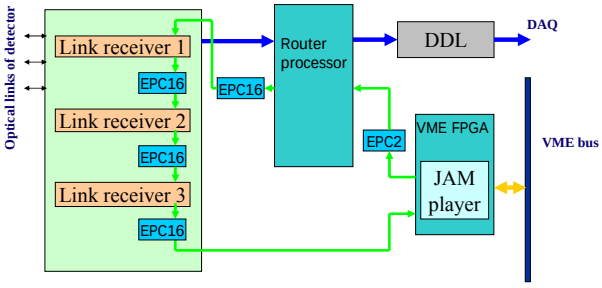

Figure 6: Altera devices on the Router in JTAG chain

C. Temperature interlock

The Router receives in the data stream from the pixel detector also temperature information of the pixel sensors and the MCMs. This information is taken from analog-digital converters which are connected to temperature sensors (Pt-1000). The deserialized temperature values are compared in the Router FPGA with the temperature limit. In case the temperature exceeds the temperature limit the Router sends temperature interlock as LVTTL signal to the low voltage power modules. One Router can monitor 6 channels i.e. temperature from 6 half-staves. One low voltage module which has one interlock input provides voltages for 6 half-staves. In case the interlock signal is active, the voltages for all 6 half-staves will be switched off.

D. TTC interface

The Router receives the trigger control signals from the ALICE Central Trigger Processor (CTP) through the on-board TTCrx chip [13] and forwards the trigger commands to the pixel detector. In the Router FPGA the L0 signal, L1 signal, L1 message, L2 message are decoded. These trigger signals and the messages are checked, aligned and stored in the trigger FIFO inside Router FPGA. In case of a trigger error the information is sent to the DAQ system in DAQ header [13]. State machines inside the Router FPGA check the number of L1 and L2 triggers and in case that there are 4 L1 triggers and no L2 trigger the Router sends the BUSY signal to ALICE CTP. All information coming from TTCrx chip is written into the dual port FIFO memory for synchronization. It is clocked with an adjusted clock produced by the PLL inside the Router FPGA. This clock is necessary for the proper trigger data registers timing. The other side of the dual port FIFO memory is clocked with the global system clock and trigger data are in this way synchronized with the main FPGA clock.

E. DAQ interface

The data are read-out from the link receivers and are stored in the FIFO memory inside the Router FPGA which is connected to DAQ interface. If the DAQ is ready, then FIFO is immediately enabled for send data to the DAQ. If the DAQ is busy then the data from the current event are stored into the FIFO memory and they are waiting in the FIFO memory until DAQ is ready. The Router creates also the DAQ header for DAQ system (8 x 32bits) which contains information from trigger messages and front-end electronics. The DAQ header is described in [13].

F. Interface between Router FPGA and link receivers

Upon receiving the L2accept trigger from ALICE CTP the Router starts to check the event ready bit in all 3 link receivers. When the event ready is active in all 3 link receivers, the Router reads 4 registers in each link receiver to get the information about the start address and the length of event stored in the link receivers and the information about errors occurred on the detector. After reading this information the Router starts the data read-out from the dual-port memory of each link receiver and merges the data from 6 channels. If the Router does not find the event ready flag after time necessary for readout in a channel, this channel will have timeout flag asserted in the DAQ header. The Router does not read data from this channel and DAQ is informed about the timeout in this channel. The errors occurred on the detector are also send in the DAQ system in the DAQ header.

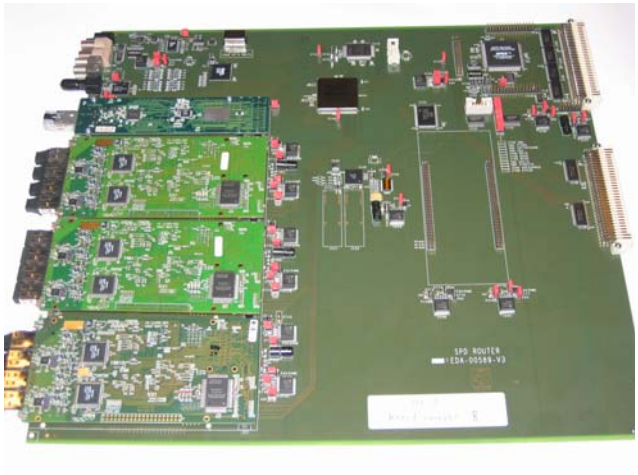

Figure 7: SPD Router

IV. INTEGRATION AND COMMISSIONING

The full SPD read out chain was successfully operated with two half staves during a joint ITS beam test in November 2004, together with a few modules of the other ITS subdetectors (silicon drift (SDD) and silicon strip (SSD)). The functionality and the interface of the off-detector electronics to the ALICE TTC, the DAQ, a simplified version of the DCS system and the on-detector electronics were verified in a combined run with SSD and SDD during 11 hours. Some 5.10^6 events were recorded without errors during this run.

The SPD detector system including the off-detector electronics is currently pre-installed in the CERN Divisional Silicon Facility (DSF) – a clean room where the full detector system is integrated and commissioned before being moved to the underground area. On Fig. 8 is shown one of two VME crate equipped with 10 SPD Routers.

Figure 8: 9U/6U VME crate with 10 final SPD Routers

V. SUMMARY

The integration of the ALICE SPD off-detector electronics with its many challenging technical developments is presented. All the off-detector electronics modules have been produced and tested with final detector elements and have proven to satisfy all specifications. Integration and commissioning of the final system are in progress.

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